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Application of quantum well-like thermocouple to thermoelectric energy harvester by BiCMOS process

S.M. Yang [a,*], M. Cong [b], T. Lee [a]

[a] Department of Aeronautics and Astronautics, National Cheng Kung University, Taiwan, ROC
[b] School of Mechanical Engineering, Dalian University of Technology, Dalian, China

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ABSTRACT

This work aims at improving the energy harvester performance by using low-dimensional thermoelectric materials. A micro-thermoelectric generator (μTEG) with quantum well-like thermocouples is developed by state-of-the-art CMOS (Complementary metal-oxide semiconductor) process. A relaxation-time model is applied to analyze the characteristic length of silicon germanium quantum well, and a thermal model is also applied to calculate the thermocouple size for optimal performance by matching the thermal/electrical resistance. Analysis based on TSMC 0.35 μm 3P3M (3-poly and 3-metal layers) BiCMOS process shows that the maximum power factor and voltage factor of a μTEG is 0.241 $\mu W/cm^2 K^2$ and 10.442 $V/cm^2 K$. Design implementation validates that the μTEG with 60 μm × 4 μm quantum well-like thermocouples (0.05 μm $Si_{0.9}Ge_{0.1}$ quantum well on 0.300 μm P-thermoleg and 0.280 μm N-thermoleg) has the best performance compared with those reported in the literature.

1. Introduction

Micro-thermoelectric generators (μTEG) have been successfully developed by CMOS process [1–3], where silicon-based design has the advantage of using thin-film process in semiconductor infrastructure for batch production. This development is a major improvement over the previous works by electrochemical thick-film deposition of V–VI thermoelectric compounds [4] and by thin-film deposition of polycrystalline silicon/germanium [5,6]. The former is incompatible to CMOS (Complementary metal-oxide semiconductor) process while the latter's bonding process may jeopardize process stability.

The efficiency of thermoelectric material is often described by a dimensionless number called the figure-of-merit ZT, $ZT = \sigma S^2 T/k$, where T is the absolute temperature, σ and k are the electrical and thermal conductivity, respectively, and S is the Seebeck coefficient. Material with high ZT is desired in thermoelectric generator design; in practice, however, it is difficult to increase ZT because increasing S often leads to simultaneous decreasing σ and increasing σ also leads to increasing k by the Wiedemann–Franz law. In bulk thermoelectric materials, Bi_2Te_3 alloys have the highest ZT at about 1.0 at 300 K and there has been only 10% increase in ZT over the three decades before 1990 because the change of one parameter adversely affects the other.

Hicks and Dresselhaus [7] renewed the interest in thermoelectric materials and showed that ZT > 2 can be achieved by low-dimensional semiconductors such as quantum well and quantum wire [8]. The breakthrough of ZT > 2.4 by Venkatasubramanian et al. [9] and ZT > 2.0 by Harman et al. [10] and Hsu et al. [11] have mainly benefited from the reduced thermal conductivity. Even with these advances, applications of low-dimensional thermoelectric materials and their integration with state-of-the-art semiconductor process have not been explored as yet.

2. Quantum well-like layer in CMOS process

For thermoelectric materials with feature size (also called the characteristic length) a < 100 nm, the quantum confinement effect and spatial confinement effect have been known to increase the figure-of-merit ZT. The former eliminates some states that the electrons can occupy, since they do not obey the boundary conditions of electronic wave function. The latter reduces the phonon relaxation rate and lowers the thermal transport properties of low-dimensional materials. In quantum wells, the electrons are confined to move in two-dimension so that the electron motion perpendicular to the potential barrier is quantized. This change of the energy band structure and electronic density-of-states (DOS) can increase the asymmetry between the hot/cold electron transport, obtain large transport energy, and increase the number of carriers in the materials, thereby achieving higher Seebeck coefficient. In addition, thermal conductivity will be reduced because of the phonon scattering at the interfaces, and the phonon dispersion

* Corresponding author. Tel.: +886 6 2389122; fax: +886 6 2389940.
E-mail address: smyang@mail.ncku.edu.tw (S.M. Yang).

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Nomenclature

A	area
a	characteristic length of the quantum well
d	depth of thermal isolative cavity
e	electron charge
F	Fermi–Dirac function
$\hbar$	Plank constant
K	thermal resistance
k	thermal conductivity
k_B	Boltzmann constant
L	length of thermocouple
m	effective mass component
N	number of thermocouple
P	specific power
R	electrical resistance
S	Seebeck coefficient
t	thickness
T	temperature
U	open-circuit voltage
W	width of thermocouple
ς	chemical potential
μ	mobility
ϕ_p	power factor
ϕ_u	voltage factor
τ	relaxation time

subscript

c	cold side
e	electron
g	thermocouple
h	hot side
n	N-thermoleg
p	P-thermoleg
ph	phonon
x	x-direction
y	y-direction
int	interface
1D	one-dimension
2D	two-dimension
3D	three-dimension

and group velocities are also changed due to spatial confinement by the boundaries [12]. The model of thermoelectric properties is based on the relaxation-time approximation [7]. The figure-of-merit ZT is defined by

$$ZT = \frac{S^2 \sigma T}{k_e + k_{ph}} \quad (1)$$

where k_e is the electronic thermal conductivity and k_{ph} is the phonon thermal conductivity. For two-dimension (2D) quantum well, the figure-of-merit can be written explicitly by [7]

$$Z_{2D}T = \frac{F_0((2F_1/F_0) - \varsigma_{2D})^2}{(1/(k_B^2 T \mu_x / 2\pi a e k_{ph})(2k_B T/\hbar^2)(m_x m_y)^{1/2}) + 3F_2 - (4F_1^2/F_0)} \quad (2)$$

where F_i is the Fermi–Dirac function, $F_i = \int_0^\infty x^i dx/(e^{(x-\varsigma_{2D}^*)} + 1)$, ς_{2D} is the reduced chemical potentials of quantum well, $\varsigma_{2D} = (\varsigma - (\hbar^2\pi^2/2m_x a^2))/k_B T$, ς is the chemical potential of bulk material, k_B is Boltzmann constant ($k_B = 1.381 \times 10^{-23}$ J/K), $\hbar$ is Plank constant ($\hbar = 1.055 \times 10^{-34}$ J s), e is electron charge ($e = 1.602 \times 10^{-19}$ C), m_x and m_y are the effective mass components, $m_x = m_y = 0.43 m_0$ and $m_0 = 9.109 \times 10^{-31}$ kg, μ_x is the mobility in x-direction, $\mu_x = e\tau/m_x = 1440\ \mathrm{cm^2/V/s}$, τ is the relaxation time, and a is the characteristic length of the quantum well. The design parameter a provides the degree-of-freedom for better thermoelectric properties in μTEG design by CMOS and/or BiCMOS process in standard IC foundry.

The fabrication process of silicon germanium (SiGe) heterojunction bipolar transistor (HBT) as shown in Fig. 1(a) is employed in the design of quantum well-like thermocouples, where the N-type emitter is poly-silicon, the P-type base is poly-SiGe, and the N-type collector (light doping) and N-type sub collector (heavy doping) are in the silicon substrate. An HBT with large band-gap difference and valence band-offset in BiCMOS process can minimize the undesired electron hole being injected from the base to the emitter so as to achieve higher emitter efficiency and current gain. The $Si_{0.9}Ge_{0.1}$ layer in the HBT base is selected for analyzing the thermoelectric properties. Figs. 2 and 3 illustrate the effect of the characteristic length on 1D (quantum wire), 2D (quantum well), and 3D (bulk) materials' thermoelectric properties predicted by the relaxation-time model [7]. In both 1D and 2D low-dimensional materials, the decrease of characteristic length a significantly increases both the Seebeck coefficient and electrical conductivity, while simultaneously decreases the thermal conductivity. The increase of electron conductivity in Fig. 2(a) and Seebeck coefficient in Fig. 2(b) comes mainly from the quantum confinement of carriers, while the decrease of the thermal conductivity in Fig. 3(a) from the spatial confinement of the acoustic phonons.

With the progress of CMOS in deep sub-micron ranges such as 45 nm and 32 nm processes, SiGe quantum wire structure becomes feasible by defining ultra-thin layer with minimum line width. Judgments on using quantum well or quantum wire can be seen in Fig. 3(b). When $a > 8$ nm, the quantum wire's ZT becomes lower due to the aggressively decreasing carrier mobility outweighs the decreasing thermal conductivity. The drop in carrier mobility at room temperature in quantum wires can also be explained by increasing electron scattering of the acoustic phonons due to spatial confinement as shown in Fig. 2(a). For example, the electron mobility in Si quantum wire is decreased from 120 $\mathrm{cm^2/V\,s}$ to < 15 $\mathrm{cm^2/V\,s}$ when its radius decreases from 2.3 nm to 1 nm [13]. Consequently, quantum well is preferable to thermoelectric applications in the range of $a > 8$ nm. SiGe quantum well of thickness from 20 nm to 100 nm as often seen in SiGe base can be uniformly grown by UHV-CVD epitaxy technique [14].

3. μTEG with quantum well-like thermocouples

TSMC 0.35 μm BiCMOS process with two poly-silicon layers, one poly-SiGe layer and three metal layers (3P3M) is adopted for the μTEG design in this work. The cross section shown in Fig. 1(b) consists of the gate poly-silicon (GPOLY), emitter poly-silicon (EPOLY), base poly-SiGe (BPOLY), aluminum (M1-3), inter-metal-oxide (IMD1-2), gate oxide (GOX), field oxide (FOX), metal contact (CO), and metal via (Via1-2) on a single crystallized silicon substrate. The μTEG design combining conventional in-plane and cross-plane design is illustrated in Fig. 4(a), in which the heat input from the top surface is confined passing through in-plane thermolegs. The thermal isolation cavity beneath the thermocouples is to minimize heat leakage and facilitate better thermoelectric conversion [2]. The patterned poly-silicon and poly-SiGe thermolegs of a thermocouple are interconnected by aluminum pads. Fig. 4(b) illustrates three interconnected thermocouples with the cold junctions on the gate oxide layer and the hot junctions on the field oxide layer. The length, width, and thickness of a thermoleg is denoted by L_g, W_g, and t_g in Fig. 4(c), and A_h and A_c are the contact area of the hot and cold junctions, respectively, and d is the cavity depth.

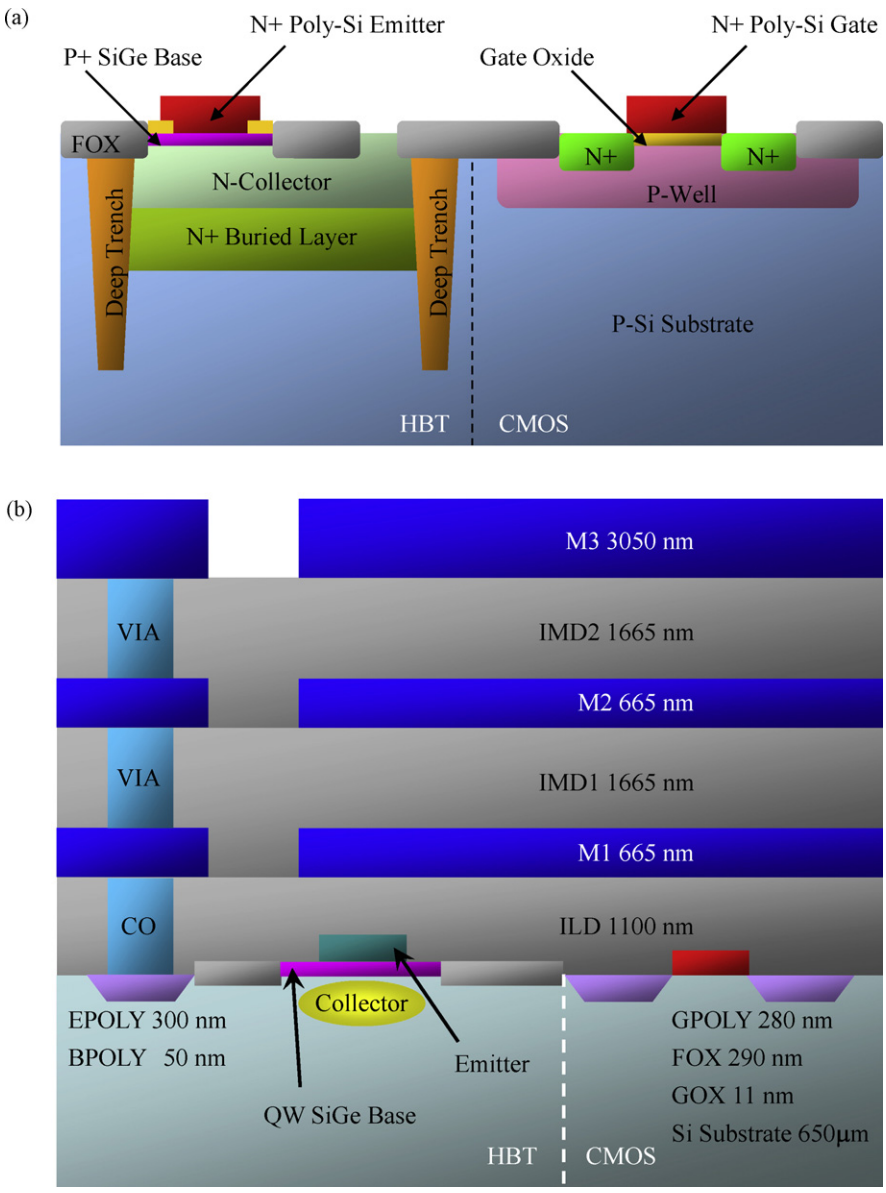

Fig. 1. (a) Illustration of SiGe structure in BiCMOS process for producing quantum well-like thermocouples and (b) cross section of the TSMC 0.35 μm 3P3M SiGe HBT BiCMOS foundry process.

For a thermocouple with hot and cold junction temperature T_h and T_c, the temperature difference $\Delta T_g = T_h - T_c$ generates an open-circuit voltage U_o, $U_o = S\Delta T_g$, where $S = S_p - S_n$ is the combined Seebeck coefficient. The open-circuit output voltage of a generator with N thermocouples is $U_o = NS\Delta T_g$. The thermal model [1,2] is employed to simulate a generator with the hot side, the thermocouple, and the cold side with thermal resistance K_h, K_g, and K_c, respectively. Previous works have been plagued by undesirable Joule heating from relative large Ohmic resistance and by negligible temperature gradient across the thermolegs from small thermal resistance. Optimal design of the thermoleg geometry for higher output power and voltage is thus necessary. The thermal and electrical resistances are determined by geometry of the thermolegs,

$$K_g = \frac{1}{N}\frac{L_g}{W_g}\left(\frac{1}{k_p t_p} + \frac{1}{k_n t_n}\right), \tag{3a}$$

$$K_h = \frac{1}{2N}\frac{t_h}{k_h A_h}, \tag{3b}$$

$$K_c = \frac{1}{2N}\frac{t_c}{k_c A_c} + K_{int}, \tag{3c}$$

$$R_g = N\frac{L_g}{W_g}\left(\frac{\rho_p}{t_p} + \frac{\rho_n}{t_n}\right). \tag{3d}$$

where L, W, t, A, K, k, and ρ is length, width, thickness, area, thermal resistance, thermal conductivity and electrical resistivity, and the indices p, n, g, h, c, and int refer to P-thermoleg, N-thermoleg, thermocouple, hot side, cold side, and interface, respectively. Note K_c also includes the interface contact resistance. μTEG performance is known strongly dependent on the thermal resistance of the interfaces during energy harvesting [15]. Precise estimation of K_{int} is difficult, and the metal–ceramic interface (1–20 cm^2 K/W) is assumed in the simulations.

Previous works in thermoelectric materials [16] with the definition of power factor in [W/cm K^2] unit emphasize more on material property (per unit length) than on device performance (per unit area.) Recent studies in energy harvesters have adopted the power factor and voltage factor $\phi_p = P/A\Delta T^2$ [W/cm^2K^2] and $\phi_u = U/A\Delta T$

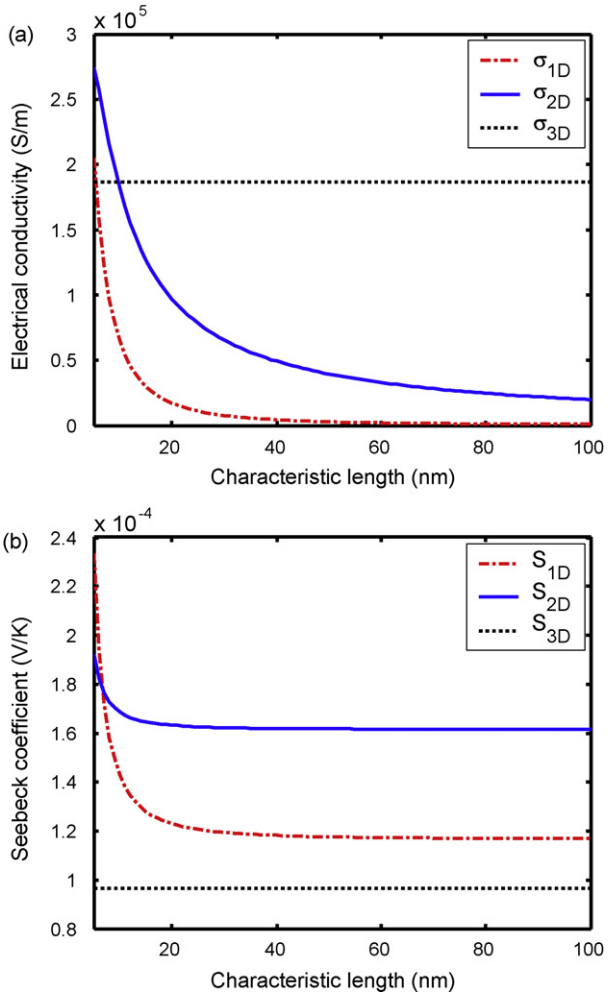

Fig. 2. (a) Electrical conductivity in (S/m) and (b) Seebeck coefficient (V/K) of $Si_{0.9}Ge_{0.1}$ quantum well at various characteristic lengths a (nm) in room temperature.

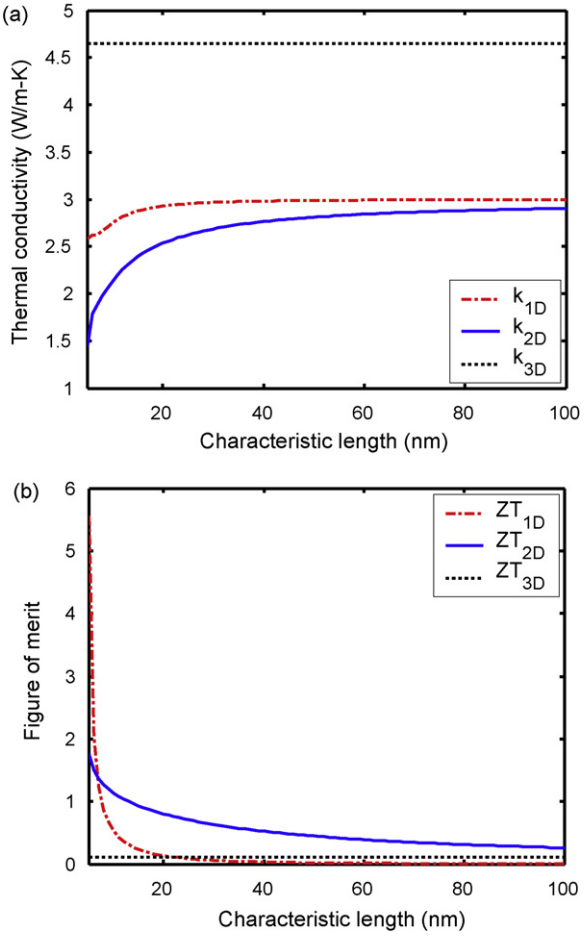

Fig. 3. (a) Thermal conductivity (W/mK) and (b) ZT of the $Si_{0.9}Ge_{0.1}$ quantum well at various characteristic lengths a (nm) in room temperature.

[V/cm^{2}K] to evaluate the generator performance per unit area [1,2,6]. In view of the thermal isolation cavity design, the temperature gradient can be effectively maintained and the power factor and voltage factor are similar to those in Refs. [1,2],

$$\phi_p = \frac{R_g}{4A\Delta T^2 N^2 S^2}\left[\frac{1}{K_c} - \frac{1}{K_h} + 2C_2\cos\left(\frac{1}{3}\arccos\left(\frac{C_1}{C_2^3}\right) + \frac{4\pi}{3}\right)\right]^2 \quad (4a)$$

$$\phi_u = \frac{R_g}{A\Delta TNS}\left[\frac{1}{K_c} - \frac{1}{K_h} + 2C_2\cos\left(\frac{1}{3}\arccos\left(\frac{C_1}{C_2^3}\right) + \frac{4\pi}{3}\right)\right]. \quad (4b)$$

where $C_1 = ((1/K_c) - (1/K_h))((1/K_c^2) + (2/K_cK_h) + (1/K_h^2) + (4/K_gK_h) + (4/K_gK_c)) + (2N^2S^2/R_g)((T_0/K_c^2) - (T_1 - T_0/K_cK_h) - (T_1/K_h^2))$, $C_2 = \sqrt{(1/K_c^2) + (2/3K_cK_h) + (1/K_h^2) + (8/3K_g)((1/K_c) + (1/K_h)) + (4N^2S^2/3R_g)((T_0/K_c) + (T_1/K_h))}$, and A is the generator area. Consider symmetric design using TSMC 0.35 μm BiCMOS process with L_g = 1–150 μm and W_g = 1–10 μm. The thin-film layer thickness are EPOLY t_p = 0.300 μm, GPOLY t_n = 0.280 μm, the oxide thickness FOX t_h = 0.290 μm on the hot side and the substrate thickness t_c = 650 μm on the cold side. The $Si_{0.9}Ge_{0.1}$ quantum well-like, low-dimensional material BPOLY is 0.050 μm thickness (characteristic length 50 nm), and the material properties of poly-silicon in standard BiCMOS process are: S_p = 103 μV/K, ρ_p = 2.21 μΩ m, S_n = −57 μV/K, ρ_n = 0.813 μΩ m, k_p = 31.2 W/mK, k_n = 31.5 W/mK, the thermal conductivity of oxide on the hot side (thickness 0.290 μm), k_i = 1.1 W/mK, and that of the silicon substrate on the cold side (thickness 650 μm), K_c = 168 W/mK. Fig. 3(b) illustrates that the figure-of-merit of the SiGe quantum well-like thermocouple at a = 50 nm is $Z_{2D}T$ = 0.566 at 300 K, which is about 4.5 times of the bulk material ($Z_{3D}T$ = 0.125) in the same figure, and it is much higher than the P- and N-poly-Si with $Z_{3D}T$ = 0.046 and 0.038 as calculated from the parameters listed above. It is thus desirable to use quantum well-like thermocouple in μTEG design. Figs. 5 and 6 illustrate the power factor and voltage factor calculated by Eqs. (4a) and (4b) for the generator with thermocouple width W_g = 4 μm and 8 μm. Numerical results indicate that the μTEG with quantum well-like thermocouple of 50 μm × 4 μm has the largest power factor 0.241 μW/cm^2 K^2 and voltage factor 10.442 V/cm^2 K. The optimal design is also at 60 μm × 8 μm. Longer L_g requires wider W_g for thermal/electrical resistance matching.

4. Design verification

Fig. 7(a) illustrates the layout of a 1500 μm × 1500 μm μTEG chip, where the test structures located around the perimeter are to measure the thermoelectric properties of the thin-film lay-

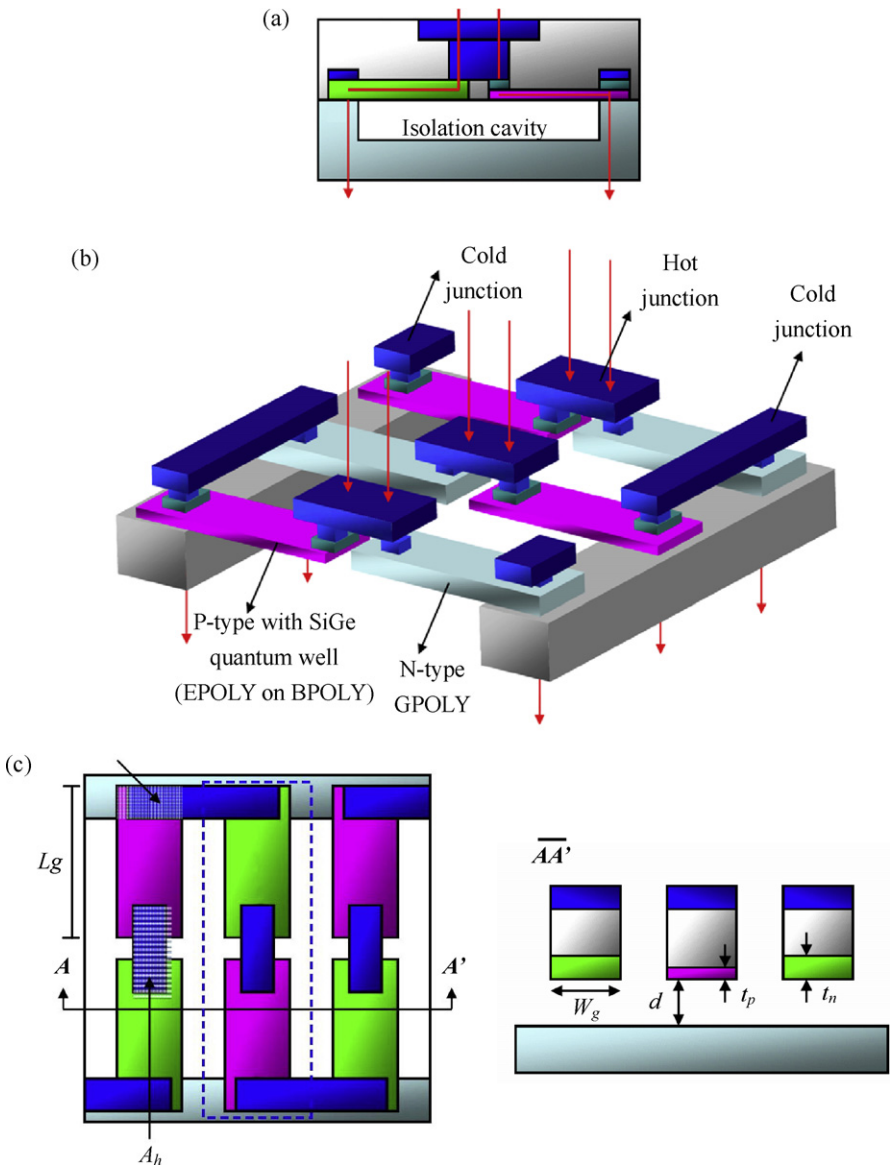

Fig. 4. (a) The μTEG design with co-planar thermocouples insulated by thermal isolation cavity, (b) the thermocouples connected electrically in series and thermally in parallel, and (c) the top view and the cross section of the μTEG indicating the geometry parameters (not to scale).

ers. μTEG of various thermocouple sizes is listed in Table 1. For post-processing consideration, the pads for electrical connection are fabricated by patterning the top metal layer into squares of 100 μm × 100 μm with 10 μm trenches around, and the metal layer M3 serves as the etching protection for the structure beneath. The post-process is shown in Fig. 7(b), where the quantum well-like thermocouples are deposited and patterned by CMOS process, followed by vertical SiO_2 etching and isotropic Si etching using the top aluminum layer as etching mask. Fig. 7(c) illustrates the SEM photo of the 20 μm × 4 μm thermocouples, and they are purposely damaged to examine the RIE etching of the 10 μm thermal isolation cavity underneath the thermocouples. The width of the etch windows for the cavity is at 4 μm, as it is limited by the aspect ratio in ICP etching. The top aluminum layer serves as the mask in post-processing to protect the thermocouple from vertical etching and to create the thermal isolation cavity. The GOX layer serves as electrical isolation at the cold junctions to prevent short-circuit of the thermocouples and the FOX layer as the protection of the thermolegs during isotropic silicon etching. The GPOLY layer serves as the N-thermolegs and the EPOLY + BPOLY layer as P-thermolegs. The M1 layer serves as interconnections of thermolegs, while the M2 and M3 layers as the etching masks during post-process and they stay as thermal conductor at the hot junctions. CO and Via1-2 layers are the interconnections. There are two challenges in improving the power factor of quantum well: (1) any low-dimensional structure may have imbedded barriers [17] which are electrically inactive thus reducing the performance by the thermal leakage between the hot/cold junctions [18], and (2) the sharp features in quantum well's density-of-state disappear quickly upon material's non-uniformity. In μTEG design, the UHV-CVD epitaxy technique is applied to produce the 50 nm $Si_{0.9}Ge_{0.1}$ base for better uniformity.

Performance of the μTEG chip is characterized by 20 °C temperature difference from a heating wire on the chip's top surface and a cold plate with thermal conductive gel on the bottom surface. The experimental setup illustrated in Fig. 5(a) is similar to that in [2]. The voltage and current are listed in Table 1. K_{int} is validated experimentally by curve fitting the simulation results in Figs. 5 and 6, and the result at about 9 cm^2 K/W falls within the metal–ceramic interface of 1–20 cm^2 K/W. The measurements show that, among the

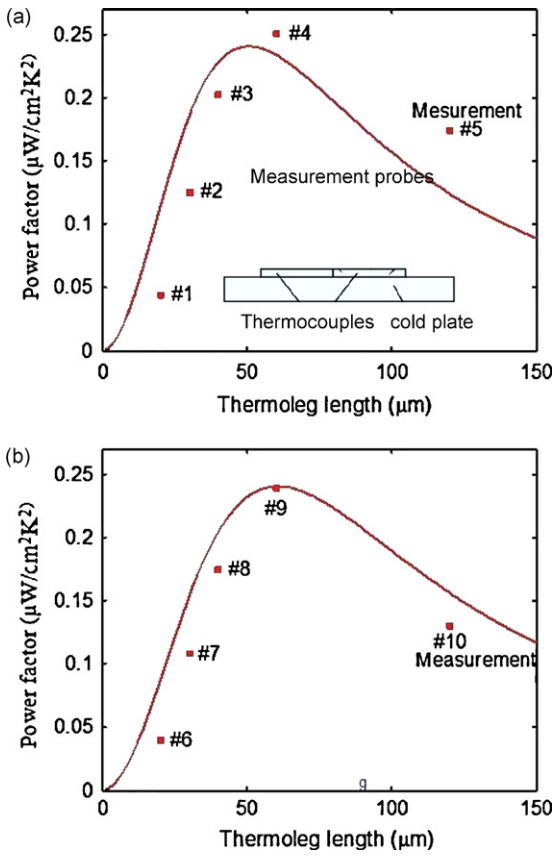

Fig. 5. Power factor simulation and measurement of the μTEG with quantum well-like thermocouples at different thermoleg length: (a) #1–#5 with W_g = 4 μm and (b) #6–#10 with W_g = 8 μm.

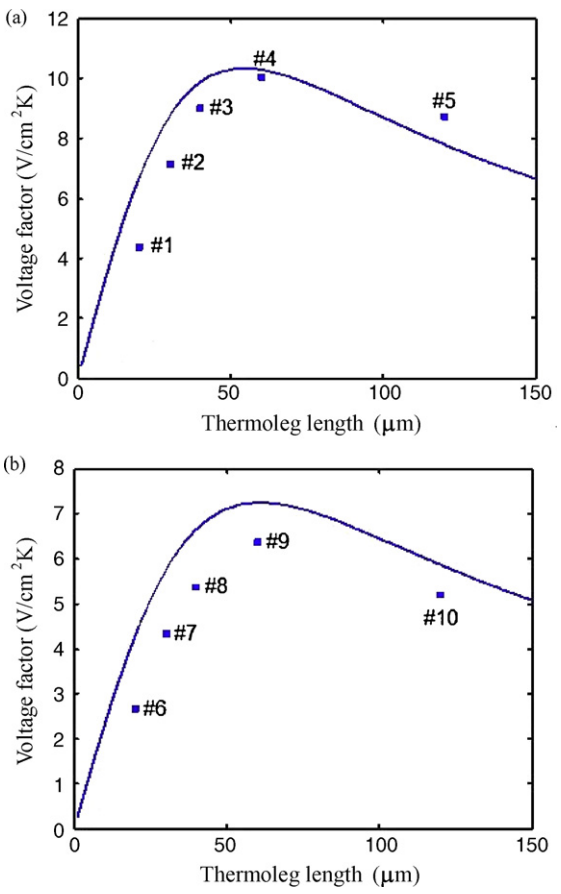

Fig. 6. (a) Voltage factor simulation and measurement of the μTEG with quantum well-like thermocouples at different thermoleg length: (a) #1–#5 with W_g = 4 μm and (b) #6 - #10 with W_g = 8 μm.

Table 1
Measurement results of the power and voltage factors of the μTEG with quantum well-like thermocouples.

μTEG	$L_g \times W_g$ (μm)	U (mV)	I (μA)	ϕ_p (μW/cm² K²)	ϕ_v (V/cm² K)
#1	20 × 4	10.5	0.4	0.0438	4.375
#2	30 × 4	17.1	0.7	0.1247	7.125
#3	40 × 4	21.6	0.9	0.2025	9.000
#4	60 × 4	24.1	1.0	0.2510	10.042
#5	120 × 4	20.9	0.8	0.1742	8.708
#6	20 × 8	6.4	0.6	0.0400	2.667
#7	30 × 8	10.4	1.0	0.1083	4.333
#8	40 × 8	12.9	1.3	0.1747	5.375
#9	60 × 8	15.3	1.5	0.2391	6.375
#10	120 × 8	12.5	1.0	0.1302	5.208

10 thermocouple sizes, 60 μm × 4 μm has the largest power factor 0.251 μW/cm² K² and voltage factor 10.042 V/cm² K. The effective size of a thermocouple pair (60 μm × 4 μm) is about 1000 μm² and, with 20 °C temperature gradient, the power harvested is about 100 μW/cm². The thermal resistance of a single thermocouple is 3.3×10^6 K/W from Eq. (3a), and that of a 1 cm² μTEG containing about 100,000 thermocouples is 33 K/W. This thermal resistance is higher than that in Huesgen et al. [6] in which the resistance is 1.555 K/W for the 120 × 40 × 0.7 μm (length × width × thickness) poly-silicon thermocouples. It should be noted that the performance of a μTEG is very sensitive to the contact resistance during measurement and to the thermal resistance within the thermocouples.

Table 2 lists the power factor and voltage factor compared with the μTEGs reported in the literature, where significant improvement is achieved by the quantum well-like thermocouples. The

Table 2
Comparison of the CMOS μTEGs reported in the literature.

Prior work	CMOS integrated?	Thermoelectric materials	Power factor ϕ_p (μW/cm² K²)	Voltage factor ϕ_v (V/cm² K)
[1]	Yes (Modified)	Poly-Si	0.0426	2.6
		Poly-SiGe	0.0352	2.2
[2]	Yes	Poly-Si	0.0417	2.417
[3]	Yes	Poly-Si	0.0427	3.417
[6]	No	Al/poly-Si	0.00363	0.746
		BiTe	0.00814	2.38
[18]	No	Al/Si	0.091	–
[19]	No	Poly-SiGe	0.0026	12.5
This work	Yes	Poly-Si + SiGe	0.251	10.042

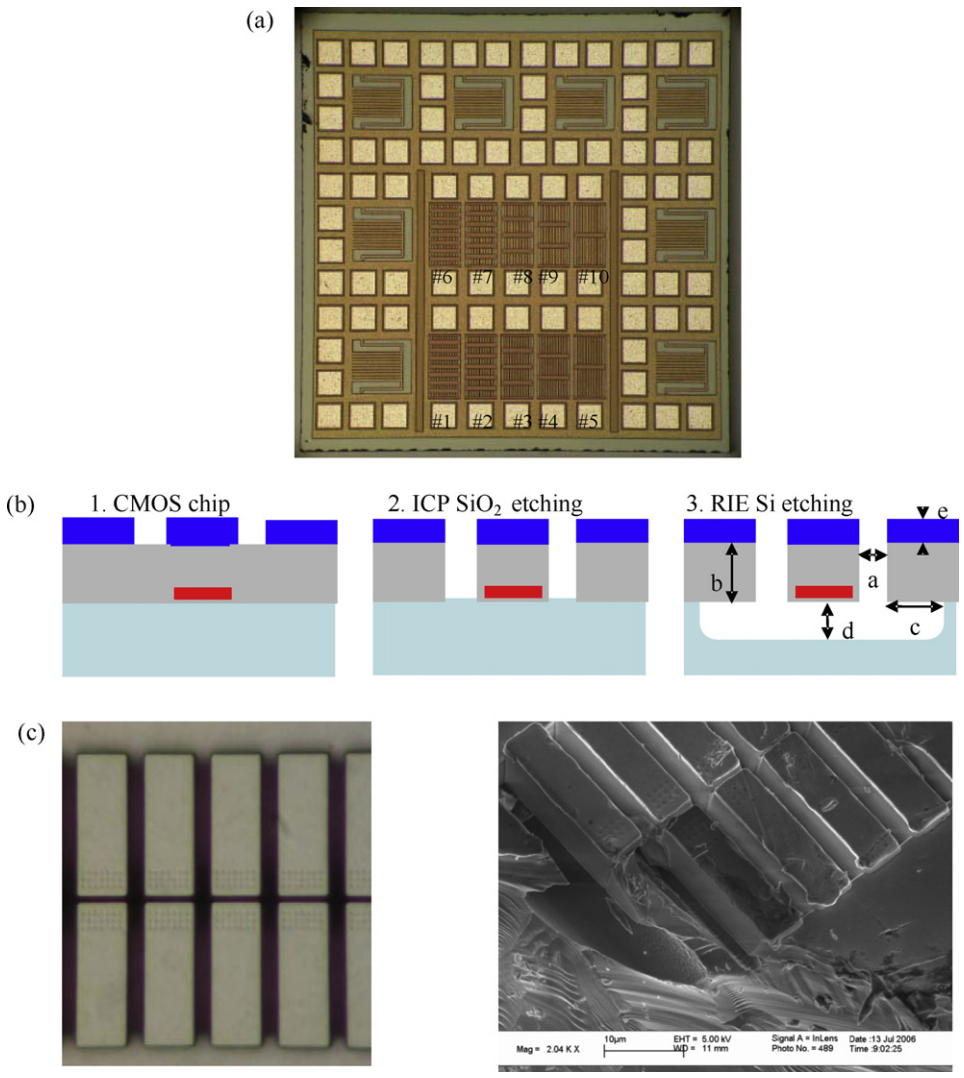

Fig. 7. (a) Photomicrograph of the μTEG chip, (b) the dry etching post-process, first by ICP for SiO_2 vertical etching and then by RIE for Si isotropic etching, with the geometry parameters (not to scale) a: width of the etching hole (4 μm), b: depth of ICP SiO_2 etching (4.43 μm), c: undercut of RIE silicon etching (5 μm), d: depth of RIE silicon etching (10 μm), and e: thickness of the top metal mask (3.05 μm), and (c) SEM photos of the 20 × 4 μm thermocouples before (left) and after (right) etching post-process, and they are purposely damaged to examine the RIE etching of the 10 μm thermal isolation cavity.

first thin-film μTEG was developed in 1999 in which the thermocouples, each of 500 μm × 7 μm, are doped silicon and aluminum to generate 1.5 μW at 10 °C temperature difference, or the power factor of 0.0091 μW/cm^2 K^2 [19]. The power factor is low, the membrane configuration with parallel thermal flow is impractical for on-chip thermal harvesting, and it is not CMOS compatible process. Recent designs using poly-silicon μTEG with power factor 0.00363 μW/cm^2 K^2 [6] and another using poly-SiGe with 0.026 μW/cm^2 K^2 [20] are at least an order smaller than this work. Their fabrication using wafer-bonding can be low-yield and unsuitable for batch manufacturing. A CMOS generator using polycrystalline silicon (poly-Si) and polycrystalline silicon germanium (poly-SiGe) thin-films was developed in [1], in which the thermolegs of 6 μm width and 18.5 μm length delivers a power factor of 0.00426 μW/cm^2 K^2. The power factor is an order smaller than this work, and the additional etching process requires a modified CMOS process and thus may jeopardize the process stability. A CMOS μTEG based on co-planar thermocouple design has improved the power factor to 0.0417 μW/cm^2 K^2 [2] and the most recent CMOS μTEG design based on stacked poly-silicon thermocouples can deliver 0.0427 μW/cm^2 K^2 [3]. This work based on quantum well-like thermocouples achieves the best performance and it is also CMOS compatible. Devices with enhanced thermoelectric performance by using low-dimensional materials are promising for energy harvesting.

5. Conclusions

(1) CMOS-based micro-thermoelectric generators (μTEG) have achieved significant progress from geometry-design point of view. This work aims at improving the μTEG performance from materal-design point of view. A μTEG combining the conventional in-plane and cross-plane designs is adopted so that the heat flux from the top to bottom surface is confined passing through the in-plane thermocouples. The design by TSMC 0.35 μm BiCMOS process with the $Si_{0.9}Ge_{0.1}$ thin-film layer (50 nm) has low-dimensional quantum well-like property and achieves better performance. The process has two poly-silicon layers, one poly-SiGe layer and three metal layers (3P3M). The gate oxide GOX layer serves as electrical isolation at the cold junctions to prevent short-circuit of the thermocouples, and the field oxide FOX layer as protection of the thermolegs during etching. The gate poly-silicon GPOLY layer serves as the N-thermolegs, and the emitter poly-silicon (EPOLY) and

the base poly-SiGe (BPOLY) layer as the quantum well-like P-thermolegs. These thin-films are deposited and patterned by BiCMOS process, followed by the post-process procedures of vertical SiO_2 etching and isotropic Si etching. A thermal model is applied to analyze the optimal thermocouple size by matching their thermal and electrical resistance. Experimental verification shows that the 1500 μm × 1500 μm μTEG chip with 60 μm × 4 μm thermocouples has the largest power factor 0.251 $\mu W/cm^2 K^2$ and voltage factor 10.042 $V/cm^2 K$. The design achieves superior generator performance compared with those in the literature. It should be noted that the performance of a μTEG is very sensitive to the contact resistance during measurement and to the thermal resistance within the thermocouples.

(2) The efficiency of thermoelectric material is described by the dimensionless figure-of-merit $ZT = \sigma S^2 T/k$, and the challenge is to have high ZT by increasing S and σ while simultaneously decreasing k. The quantum confinement effect and spatial confinement effect can increase ZT significantly by higher electrical conductivity and Seebeck coefficient, while the spatial confinement effect by the phonons scattered at the boundaries also reduces the thermal conductivity. A relaxation-time model is applied to analyze the characteristic length of the $Si_{0.9}Ge_{0.1}$ quantum well. Analysis shows that the ZT in characteristic length $a = 50$ nm is $Z_{2D}T = 0.566$ at 300 K, about 4.5 times of the bulk material. This figure-of-merit is also much higher than the P- and N-poly-Si, and such improvement is critical to μTEG development.

(3) One may argue that the multi-layer thin-films may not fall in the "classical" definition of a quantum well as in Refs. [7–11], but analysis of the 50 nm SiGe in BiCMOS process did show better performance in the quantum well-like thermocouples. Note that further study is required to validate experimentally the numerical results in Figs. 2 and 3, and more work in measuring the Seebeck coefficient, electrical and thermal conductivities at different temperature may be necessary. The extension of quantum well is to quantum wires and quantum dots [21,22]. Though numerical studies predict even higher ZT in quantum wires and dots due to additional electron confinement, experimental verifications has never been reported as yet as they are even more challenging.

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Biographies

S.M. Yang received his PhD degree from the University of California at Berkeley, USA, in 1988. He joined the faculty of the National Cheng Kung University, Taiwan in 1989, where he is currently a Professor in the Department of Aeronautics and Astronautics. His research interests are in smart structure systems, digital signal processing, and microsystem applications.

M. Cong received his PhD in mechanical engineering from Shanghai Jiao Tong University, Shanghai, China, in 1995, and he has been with the School of Mechanical Engineering, Dalian University of Technology, Dalian, in China, where he is presently a Professor. He was a Visiting Professor to the Department of Aeronautics and Astronautics, National Cheng Kung University, Taiwan in 2006. His interests are in mechanical systems and automation.

T. Lee received his BS, MS, and PhD degree in the Department of Aeronautics and Astronautics from the National Cheng Kung University, Taiwan, in 2001, 2003 and 2008, respectively. His research interests are in design and fabrication of CMOS Microsensors. He is also a member of the National Nano Devices Laboratory (NDL), Taiwan.